

WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a cell array consisting of a number of memory cells;

5 a bit line sense amplifier connected to the memory cell through a bit line, for sensing data of the memory cell;

a bit line equalization circuit for equalizing the bit line sense amplifier with the same voltage level;

a sense amplifier I/O line electrically connected to the bit line according to a column signal;

10 a sense amplifier I/O line equalization circuit for equalizing the sense amplifier I/O line with the same voltage level;

a local I/O line electrically connected to the sense amplifier I/O line according to a row matrix signal;

15 a local I/O line equalization circuit for equalizing the local I/O line with the same voltage level; and

an I/O sense amplifier connected to the local I/O line, for sensing and outputting the data sensed through the bit line sense amplifier,

20 wherein the bit line and the sense amplifier I/O line are equally precharged with voltages that are independently supplied through different supply lines by the bit line equalization circuit and the sense amplifier I/O line equalization circuit that are operated by an inverse signal of the row matrix signal.

2. The semiconductor memory device of claim 1, wherein the voltages are generated through different voltage generators, respectively.

3. The semiconductor memory device of claim 1, wherein the voltages
5 are generated through the same voltage generator.

4. A semiconductor memory device including a bit line, a bit line sense amplifier for sensing data of a memory cell through the bit line, a sense amplifier I/O line electrically connected to the bit line according to a column
10 signal, a local I/O line electrically connected to the sense amplifier I/O line according to a row matrix signal, and an I/O sense amplifier for outputting the data sensed through the bit line sense amplifier through the local I/O line,

wherein both ends of the bit line and the sense amplifier I/O line are precharged with the same voltage level by means of voltages that are
15 independently supplied through different supply lines.

5. The semiconductor memory device of claim 4, wherein the voltages are generated through different voltage generators, respectively.

20 6. The semiconductor memory device of claim 4, wherein the voltages are generated through the same voltage generator.